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| **LESSON PLAN** | |
| **Name of the Faculty** | **Mr. Virender Singh Rawat** |
| **Discipline** | **COMPUTER ENGINEERING** |
| **Semester** | **IV** |
| **Subject** | **COMPUTER ORGANIZATION & ARCHITECTURE** |
| **Lesson Plan Duration** | **15 WEEKS** |

\*\* Work Load (Lecture/Practical) per week (in hours): Lecture-04

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| WEEK | Theory | |
| **Lecture Day** | **Topic(Including Assignment and Test)** |
| 1st | 1st | A brief overview of the subject “Computer organization“. |
| 2nd | CPU Organization: Concept of Registers |
| 3rd | General Register Organization |
| 4th | Stack Organization |
| 2nd | 5th | Concept of Instruction Format |
| 6th | Types of instructions |
| 7th | Types of instructions |
| 8th | Concept of RISC instruction |
| 3rd | 9th | Concept of CISC instruction |
| 10th | Addressing modes :Immediate |
| 11th | Register, Direct, Indirect mode |
| 12th | Relative and Indexed mode |
| 4th | 13th | Revision |
| 14th | Class test |
| 15th | Concept of Memory Organization |
| 16th | Memory types |
| 5th | 17th | Memory Hierarchy |
| 18th | ROM and RAM Chips |
| 19th | Concept of Memory Address Map |
| 20th | Connections of Memory Chips with the CPU |
| 6th | 21st | Concept and usage of Auxiliary Memories and types |
| 22nd | Revision |
| 23rd | Study of Magnetic Disks ,Magnetic Tapes |
| 24th | Associative and Cache memory |
| 7th | 25th | Concept of Virtual Memory |
|  | 26th | Concept of Memory Management Hardware |
|  | 27th | Read and Write Operation |
|  | 28th | Revision |

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| 8th | 29th | Test |
| 30th | Concept of Input/output Organization |
| 31st | Basic Input output System BIOS and its Function |
| 32nd | Oral test |
| 9th | 33rd | Testing and Initialization by BIOS |
| 34th | Configuring the System |
| 35th | Different modes of Data Transfer: Programmed I/O |
| 36th | Concept of Synchronous and Asynchronous Data, Transfer Modes |
| 10th | 37th | Concept of Interrupt Initiated Data transfer modes |
| 38th | Concept of DMA Transfer |
| 39th | Revision |
| 40th | Class test |
| 11th | 41st | Concept of Multi Processor Systems |
| 42nd | Parallel Processing and Pipe Lines |
| 43rd | Basic Characteristics of Multiprocessor |
| 44th | General purpose multiprocessors. |
| 12th | 45th | Concept of Interconnection Networks |
| 46th | Concept of Time Shared Common Bus |
| 47th | Concept of Multiport Memory, Cross Bar Switch |
| 48th | Hyper cube structures |
| 13th | 49th | Revision |
| 50th | Input-Output Interface |
| 51st | Methods of Asynchronous Data transfer |
| 52nd | Synchronous Data Transfer |
| 14th | 53rd | Strobe Control |
| 54th | Handshaking |
| 55th | Asynchronous Serial Transfer |
| 56th | Revision |
| 15th | 57th | Revision |
| 58th | Revision |
| 59th | Revision |
| 60th | Revision |